In the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently Amended) A semiconductor memory device comprising:

an array of memory cells arranged in rows and columns;

means for selecting, for testing, the memory cells of the array in a repair unit in a test operation mode;

means for supplying a power voltage to the memory cells selected for testing in the test operation mode, and turning off power to remaining memory cells not selected for testing in the test operation mode;

means for measuring standby current of the memory cells selected for testing while in the test operation mode; and

means for restoring power voltage to memory cells not selected for testing, in a normal operation mode,

wherein in the test operation mode, whether or not the selected memory cells comprise a memory cell having standby current failure is judged depending on variation of the power voltage.

2. (Original) The semiconductor memory device of claim 1, wherein the memory cells of the array are repaired in a row unit.

3. (Original) The semiconductor memory device of claim 2, wherein the selection means selects the memory cells of the array in the repair unit in response to a row address in the test operation mode.

4. (Original) The semiconductor memory device of claim 2, wherein the power voltage supplying means comprises a fuse.

5. (Canceled)

6. (Currently Amended) The semiconductor memory device of claim [[5]] 4, wherein the fuse of the power supplying means is cut when the selected memory cells comprise the memory cell causing the standby current failure.

7. (Original) The semiconductor memory device of claim 2, wherein the memory cells of the array are repaired in a column unit.

8. (Original) The semiconductor memory device of claim 7, wherein the selection means selects the memory cells of the array in the repair unit in response to a column address in the test operation mode.

9. (Original) The semiconductor memory device of claim 8, wherein the power voltage supplying means comprises a fuse.

10. (Canceled).

11. (Currently Amended) The semiconductor memory device of claim [[10]] 9, wherein the fuse of the power voltage supplying means is cut when the selected memory cells comprise the memory cell having the standby current failure.

12. (Currently Amended) A semiconductor memory device comprising:

a pad for receiving a power voltage;

a first power line connected to the pad;

a plurality of repair units, each of the plurality of repair units comprising an array of memory cells arranged in rows and columns;

a plurality of second power lines, each of the plurality of second power lines connected to a corresponding repair unit;

a selection circuit for outputting selection signals for selecting for testing the memory cells corresponding to one of the repair units in response to a row address in a test operation mode; and

a switch circuit operating in response to the selection signals, for connecting the second power line connected to the memory cells selected for testing with the first power line and disconnecting remaining second power lines from the first power line, in the test operation mode such that power is turned off from the memory cells not selected for testing and in a normal operation mode, power is restored to the memory cells not selected for testing.

wherein in the test operation mode, whether or not the selected memory cells comprise the memory cell having standby current failure is judged depending on variation of the power voltage.

13. (Original) The semiconductor memory device of claim 12, wherein the switch circuit comprises a fuse.

14. (Canceled)

15. (Currently Amended) The semiconductor memory device of claim [[14]] 12, wherein the fuse of the switch circuit is cut when the selected memory cells comprise the memory cell having the standby current failure.

16. (Original) The semiconductor memory device of claim 12, further comprising a precharge circuit for precharging the columns.

17. (Original) The semiconductor memory device of claim 16, wherein the precharge circuit is inactivated during the test operation mode.

18. (Currently Amended) A semiconductor memory device comprising:

a pad for receiving a power voltage;

a first power line connected to the pad;

a plurality of repair units, each of the plurality of repair units comprising an array of memory cells arranged in rows and columns;

a plurality of second power lines, each of the plurality of second power lines connected to a corresponding repair unit;

a selection circuit for outputting selection signals for selecting for testing the memory cells corresponding to one of the repair units in response to a column address in a test operation mode; and

a switch circuit operating in response to the selection signals, for connecting the second power line connected to the memory cells selected for testing with the first power line and disconnecting the remaining second power lines from the first power line, in the test operation mode such that power is turned off from the memory cells not selected for testing and in a normal operation mode, power is restored to the memory cells not selected for testing,

wherein in the test operation mode, whether or not the selected memory cells comprise a memory cell having standby current failure is judged depending on variation of the power voltage.

19. (Original) The semiconductor memory device of claim 18, wherein the switch circuit comprises a fuse.

20. (Canceled)

21. (Currently Amended) The semiconductor memory device of claim [[20]] 18, wherein

the fuse of the switch circuit is cut when the selected memory cells comprise the memory cell having the standby current failure.

22. (Original) The semiconductor memory device of claim 18, further comprising a precharge circuit for precharging the columns.

23. (Original) The semiconductor memory device of claim 22, wherein the precharge circuit is inactivated during the test operation mode.

24. (Currently Amended) A semiconductor memory device comprising:

a plurality of repair units, each of the plurality of repair units comprising an array of memory cells arranged in rows and columns;

first and second pads for respectively receiving a power voltage;

a first power line electrically connected to the first pad;

a second power line electrically connected to the second pad;

a first switch circuit for selectively connecting the first and second power lines in response to a test operation mode signal;

a plurality of third power lines, each of the plurality of third power lines electrically connected to a corresponding repair unit;

a selection circuit for selecting for testing the memory cells of the array in one of the repair units in a test operation mode; and

a second switch circuit for connecting the second power line to the third power line

connected to the memory cells selected for testing and disconnecting the remaining third power lines from the second power line, in the test operation mode such that power is turned off from the memory cells not selected for testing and in a normal operation mode, power is restored to the memory cells not selected for testing,

wherein in the test operation mode, whether the selected memory cells comprise the memory cell having standby current failure is judged depending on variation of the power voltage.

25. (Original) The semiconductor memory device of claim 24, wherein the second switch circuit comprises a fuse.

26. (Canceled)

27. (Currently Amended) The semiconductor memory device of claim [[26]] 24, wherein the fuse of the second switch circuit is cut when the selected memory cells comprise the memory cell having the standby current failure.

28. (Currently Amended) A semiconductor memory device comprising:

a first power line for receiving a power voltage;

a plurality of repair units, each of the plurality of repair units comprising an array of memory cells arranged in rows and columns;

a selection circuit for outputting selection signals for selecting for testing the rows in one

of the repair units in response to a row address;

second power lines, each of the second power lines common-connected to the memory cells of a corresponding repair unit; and

a switch circuit for connecting one of the second power lines to the first power line in response to the selection signals, in a test operation mode such that power is turned off from the rows of memory cells not selected for testing and in a normal operation mode, power is restored to the memory cells not selected for testing,

wherein the switch circuit comprises switches, each of the switches connected to a corresponding second power line, wherein each of the switches comprises:

a NOR gate for receiving the control signal and a corresponding selection signal, and

a PMOS transistor for connecting the first power line with a corresponding second power line in response to an output signal of the NOR gate.

29. (Original) The semiconductor memory device of claim 28, further comprising first and second pads for respectively receiving the power voltage.

30. (Original) The semiconductor memory device of claim 29, wherein the first power line is directly connected to the second pad and is connected to the first pad through a switch transistor.

31. (Currently Amended) ~~The semiconductor memory device of claim 30,~~ A semiconductor memory device comprising:

a first power line for receiving a power voltage;

a plurality of repair units, each of the plurality of repair units comprising an array of memory cells arranged in rows and columns;

a selection circuit for outputting selection signals for selecting for testing the rows in one of the repair units in response to a row address;

second power lines, each of the second power lines common-connected to the memory cells of a corresponding repair unit; and

a switch circuit for connecting one of the second power lines to the first power line in response to the selection signals, in a test operation mode such that power is turned off from the rows of memory cells not selected for testing and in a normal operation mode, power is restored to the memory cells not selected for testing; and

first and second pads for respectively receiving the power voltage,

wherein the first power line is directly connected to the second pad and is connected to the first pad though a switch transistor, and

wherein the switch transistor is controlled by a control signal that is based on whether the semiconductor memory device is in the test operation mode.

32. (Original) The semiconductor memory device of claim 28, wherein the first power line is connected to a pad for receiving the power voltage.

33. (Canceled)

34. (Currently Amended) The semiconductor memory device of claim [[33]] 28, wherein each of the switches further comprises a fuse connected between the PMOS transistor and a corresponding second power line.

35. (Original) The semiconductor memory device of claim 34, wherein in the test operation mode, whether the memory cells of the selected rows comprise the memory cell having standby current failure is judged depending on variation of the power voltage.

36. (Original) The semiconductor memory device of claim 35, wherein each of the fuses is cut when the memory cells of corresponding rows comprise the memory cell having the standby current failure.

37. (Original) The semiconductor memory device of claim 28, further comprising a precharge circuit for precharging the columns.

38. (Original) The semiconductor memory device of claim 37, wherein the precharge circuit is inactivated during the test operation mode.

39. (Currently Amended) A semiconductor memory device comprising:

a first power line for receiving a power voltage;

a plurality of repair units, each of the plurality of repair units comprising an array of memory cells arranged in rows and columns;

a selection circuit for outputting selection signals for selecting for testing the columns in one of the repair units in response to a column address;

second power lines, each of the second power lines common-connected to the memory cells of a corresponding repair unit; and

a switch circuit for connecting one of the second power lines to the first power line in response to the selection signals and disconnecting the remaining second power lines from the first power line, in a test operation mode such that power is turned off from the rows of memory cells not selected for testing and in a normal operation mode, power is restored to the memory cells not selected for testing,

wherein the switch circuit comprises switches, each of the switches connected to a corresponding second power line, wherein each of the switches comprises:

a NOR gate for receiving the control signal and a corresponding selection signal, and

a PMOS transistor for connecting the first power line with a corresponding second power line in response to an output signal of the NOR gate.

40. (Original) The semiconductor memory device of claim 39, further comprising first and second pads for respectively receiving the power voltage.

41. (Original) The semiconductor memory device of claim 40, wherein the first power line is directly connected to the second pad and is connected to the first pad through a switch transistor.

42. (Currently Amended) ~~The semiconductor memory device of claim 41,~~ A semiconductor memory device comprising:

a first power line for receiving a power voltage;

a plurality of repair units, each of the plurality of repair units comprising an array of memory cells arranged in rows and columns;

a selection circuit for outputting selection signals for selecting for testing the rows in one of the repair units in response to a row address;

second power lines, each of the second power lines common-connected to the memory cells of a corresponding repair unit; and

a switch circuit for connecting one of the second power lines to the first power line in response to the selection signals, in a test operation mode such that power is turned off from the rows of memory cells not selected for testing and in a normal operation mode, power is restored to the memory cells not selected for testing; and

first and second pads for respectively receiving the power voltage,

wherein the first power line is directly connected to the second pad and is connected to the first pad though a switch transistor, and

wherein the switch transistor is controlled by a control signal that is based on whether the semiconductor memory device is in the test operation mode.

43. (Original) The semiconductor memory device of claim 39, wherein the first power line is connected to a pad for receiving the power voltage.

44. (Canceled)

45. (Currently Amended) The semiconductor memory device of claim [[44]] 39, wherein each of the switches further comprises a fuse connected between the PMOS transistor and a corresponding second power line.

46. (Original) The semiconductor memory device of claim 45, wherein in the test operation mode, whether the memory cells of the selected columns comprise the memory cell having standby current failure is judged depending on variation of the power voltage.

47. (Original) The semiconductor memory device of claim 46, wherein each of the fuses is cut when the memory cells of corresponding columns comprise the memory cell having the standby current failure.

48. (Original) The semiconductor memory device of claim 39, further comprising a precharge circuit for precharging the columns.

49. (Original) The semiconductor memory device of claim 48, wherein the precharge circuit is inactivated during the test operation mode.

50. (Canceled)

51. (Currently Amended) A semiconductor memory device comprising:

a first power line for receiving a power voltage;

a plurality of repair units, each of the plurality of repair units comprising an array of memory cells arranged in rows and columns;

second power lines, each of the second power lines common-connected to the memory cells of a corresponding repair unit;

a selection circuit for outputting selection signals for selecting for testing one of the repair units; and

a switch circuit for connecting one of the second power lines to the first power line in response to the selection signals, in a test operation mode such that power is turned off from the repair units of memory cells not selected for testing and in a normal operation mode, power is restored to the memory cells not selected for testing; and

first and second pads for respectively receiving the power voltage,

wherein the first power line is directly connected to the second pad and is connected to the first pad though a switch transistor, and

wherein the switch transistor is controlled by a control signal that is based on whether the semiconductor memory device is in the test operation mode.

52. (Canceled)

53. (Canceled)

54. (Canceled)

55. (Currently Amended) The semiconductor memory device of claim [[54]] 51, wherein the switch circuit comprises switches, each of the switches connected to a corresponding second power line, wherein each of the switches comprises:

a NOR gate for receiving the control signal and a corresponding selection signal; and

a PMOS transistor for connecting the first power line with a corresponding second power line in response to an output signal of the NOR gate.

56. (Original) The semiconductor memory device of claim 55, wherein each of the switches further comprises a fuse connected between the PMOS transistor and a corresponding second power line.

57. (Original) The semiconductor memory device of claim 51, wherein in the test operation mode, whether the memory cells of the selected repair unit comprise the memory cell having standby current failure is judged depending on variation of the power voltage.

58. (Original) The semiconductor memory device of claim 56, wherein each of the fuses is cut when the memory cells of corresponding columns comprise the memory cell having the standby current failure.